

A NOVEL UNIVERSAL DIGITAL CONFIGURABLE POWER CONTROL AND POWER MANAGEMENT SIGNAL-MIXED SoC CONTROLLER PLATFORM FOR LIGHTING APPLICATIONS

by

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Introduction

This paper presents a new concept for digital power control and management implemented in a mixed-signal SoC (system on chip) platform based on multiple smart configurable logic engines. This controller platform is aimed for the broad power conversion industry, including: Power Supplies for Telecom, Computers and Peripherals, Consumer Electronics, Merchant SMPS (switch mode power supply) and charges, Lighting, Motor Control, Building & Home Automation, Automotive, etc.. Principally this platform was conceived to allow a complete migration path from analog to digital control in applications in which the advantages of the digital technology prevail.

This SoC controller platform named the IDC2XXX (Integrated Digital Control) was designed as a universal concept to overcome the actual limitations like latency, limited bandwidth and hard design of the existing digital approach that prevents the transition from the analog to the digital technology in the preferred applications.

Furthermore, this platform has features like minimal latency influence, fast control, broad bandwidth and high resolution that are normally envisioned as being only provided by ASIC solutions, while at the same time provides an unsurpassed time to market and the cost effectiveness required by the market.

The paper will show a scalable SoC controller platform composed of configurable logic engines - building blocks. The logic blocks' and their interconnection configurability allow this platform to match the desired power topology application and to implement all the requested control algorithms and operational functions by defining a set of constants that determine: the interconnectivity of the configurable control engines, the sequential pulses structure of the PSG (Pulse Sequence Generator) output drive signals and their interrelated timing and define the Input/Output pins. This concept allows implementing almost any type of power control and power management algorithms needed to achieve the optimal functioning and targeted performance of the end product, with practically negligible spare silicon content. In lighting, for example, this controller allows implementing any type of dimming and adapting ballast to different types of lamps without change of capacitors, resistors and magnetics.

Proprietary GUI (graphical user interface) design tools named PDK™ (parameter development kit) and PowerScene™ carry out the configuration of the digital SoC controller architecture without code programming by simple selection and tuning, most of them on-the-fly, fix engineering parameters to adapt the controller to the targeted power topology, define new algorithms and cause product to operate at optimal performance at an unsurpassed pace and sometimes in a matter of minutes.

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IDC2XXX: Main Outstanding Benefits

Feature	Value	Features achieved by
SOC for Control and Management for almost all Switching Power Machines	Almost all	11 channels of optionally controlled Interlink loops
Short and Easy Development and Debugging Time	Short & Easy	Over 50 Configurable Parameters per Channel
Fast and Easy to Modify, Update and Upgrade	Fast & Easy	Configurable Inter-connectivity
Allows implementation of almost all known topologies	Almost all	Up to 16 states Event Driven Configurable State Machine (per channel) for generation of Sequential Switching Drive Signal
Allows Creation of new topologies	New	
Allows Creation of almost any Sequence drive signal - up to 16 states per cycle	Almost any	On-the-fly configuration by CPU
Allows on-the-fly modification and adaptation of control algorithms (gains, sequence, ...) in response to external or internal event or condition (Load Current, Load Voltage, Input Voltage, Temperature, User Request, ...)	On-the-fly	Configurable Modular Software PC Wizard Software PDK Tool for creation, modification and on-the-fly configuration of the desired application.
Programmable Power Management controlled by software	Programmable	Up to 200nS Updating Calculation Time of each controlled loop Digital Filters
Fast Transient Response	Fast	Analog Signal Sampling at Low Noise Time Interval
Stable Dynamic Response	Stable	
High Noise Immunity	High	

Abbreviations appearing in the above and below tables

DSP – digital signal processor	PWM – pulse width modulation
I/O - input/output	VRD – voltage regulator down
PIDF - proportional integral differential feed-forward	VRM - voltage regulator module

IDC2XXX Applications

Market Niches

Power Supplies
AC to DC Inverters
DC to AC Inverters
Motor Control
UPS
Lighting
Home Automation
Car applications
Almost any known Power Switching Machine

Topologies

Push Pull
Half Bridge
3 Phase Bridge
Fly-back
Boost
Buck
Resonant
Quasi Resonant
Multiphase Buck
Almost any Combination of above topologies
Other known and new topologies

Cycle Time Regime

Constant frequency of PWM
Constant frequency of PWM
Constant On Time PWM
Constant Off Time PWM
Frequency Modulation
Variable On & Off
Pulse Skipping
.....
Multiple Regimes
Up to 16 states per each cycle
Alternate Time Regime - by Internal or External Events
Almost any known or requested Sequential Signal

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Functional Partitioning of the IDC2XXX Architecture

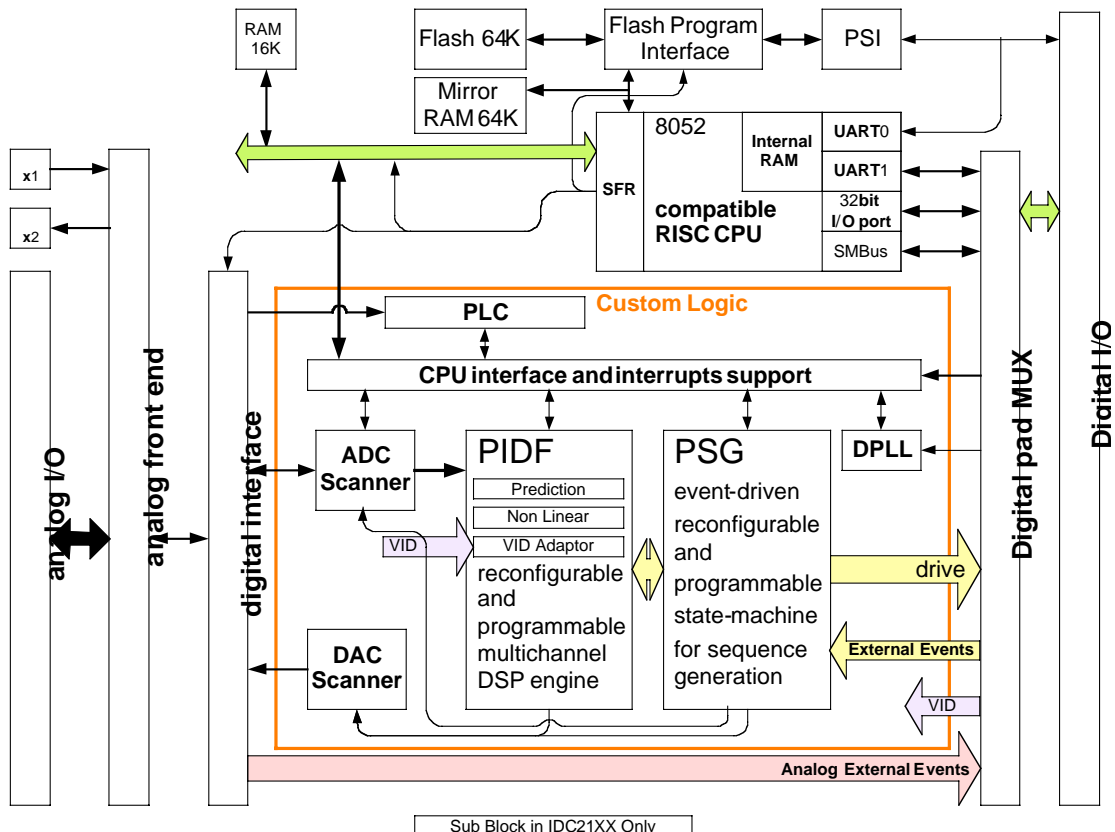
The following list shows the architecture design concept of the presented SoC IDC2XXX:

- Single chip solution - All power control and power management in a single SoC
- Configurable architecture
- All measurements and calculation by logic building blocks
- All control loops are processed in digital building blocks
- All the power sequential drivers signal are generated by building blocks
- All power switches and drivers are outside the SoC
- Differential analog section structure for high noise immunity
- Multipurpose Digital I/O

IDC2XXX Block Diagram

Abbreviations appearing in the following diagram

ADC - Analog to Digital Converter	PSG - Pulse Sequence Generator
DAC - Digital to Analog Converter	PSI – programming serial interface
DPLL – digital phase lock loop	



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IDC2XXX Architecture Structure Explanation

Immediately after connecting supply voltage to SoC (1.8V and 3.3V) the CPU loads the Custom Logic with the desired application configuration, storing in Flash Memory or a ROM according to the desired implementation. Most of the Custom Logic configurable parameters can be modified (updated) during operation (on-the-fly) in order to adapt to changes in the operating conditions (Load change, Supplied voltages change, etc.).

The Custom Logic contains all the required building blocks for closing the control loop and the generation of driving signals required by almost any known switching power machine. Each building block has configurable parameters for adapting its behavior to the implemented application.

The IDC2XXX in its large version has 11 closing loop control and signal generators for creating 11 switching sequential drive signals or signal pairs. Each of the channels comprises over 50 configurable parameters.

The IDC2XXX architecture is composed of configurable Building Blocks as mentioned above and can be configured and interconnected according to designer needs to create his own solution.

The IDC2XXX building blocks are described as follows (and for the sake of brevity only some essential configurable parameters are referred to).

Analog Front-end

Includes the following elements and their functions: ADC, DAC – generating analog reference to analog comparators, Track and Hold units (T&H) – enable sampling of analog input at certain timing in relation to switching drive signals, Invert Amplifier – allows sampling of negative signal, Variable Gain Amplifier – keeps high resolution for small signal, Differential Amplifier – for achieving high noise immunity, Analog Comparators – for creating events used in generation of some drive signals, for example current mode control.

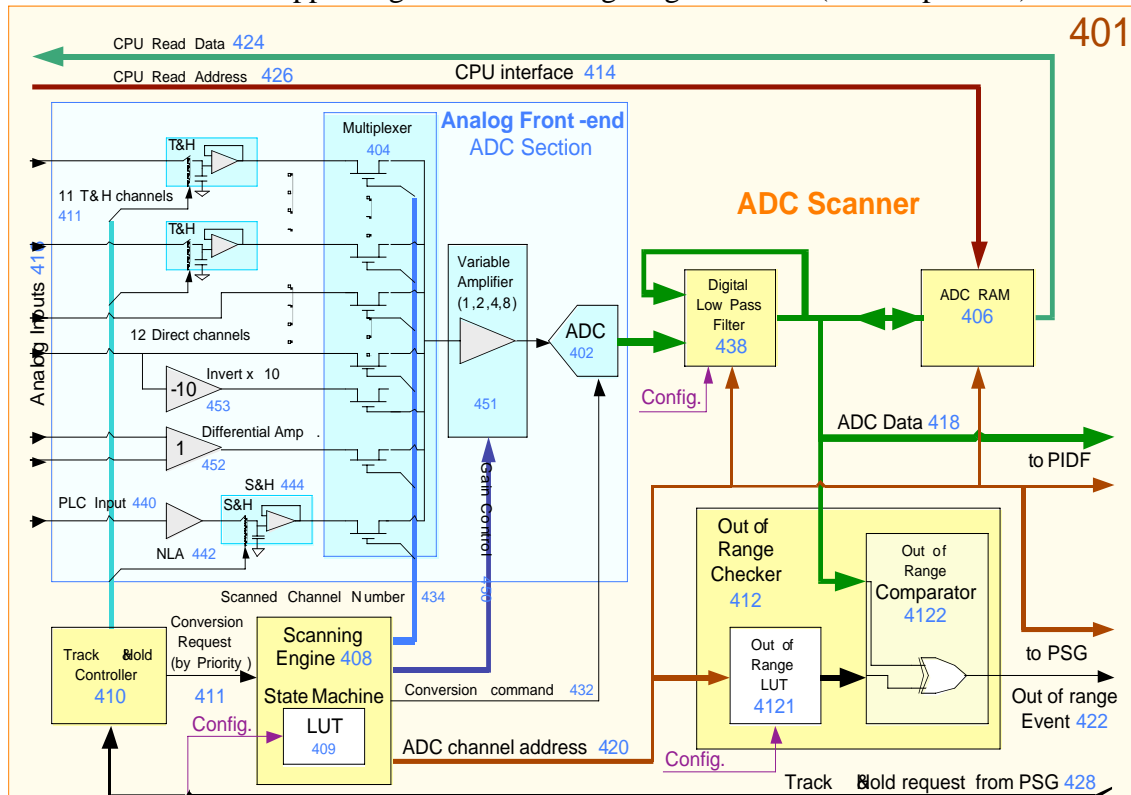
The ADC and associate elements are commanded by the ADC Scanner (via digital interface) for the sampling rate and sequence of the analog inputs like Analog feedback signals, other sensing of voltages, currents, temperatures etc. and converting to digital data by the ADC. The ADC Scanner includes Digital Filter for noise rejection, RAM for all inputs converted data (each input has its own address) used for filtering operation and enabling software monitoring. The data in the RAM is updated whenever the related analog input is sampled.

The DAC and its associate elements are commanded by the DAC Scanner for creating the required references to the analog comparators.

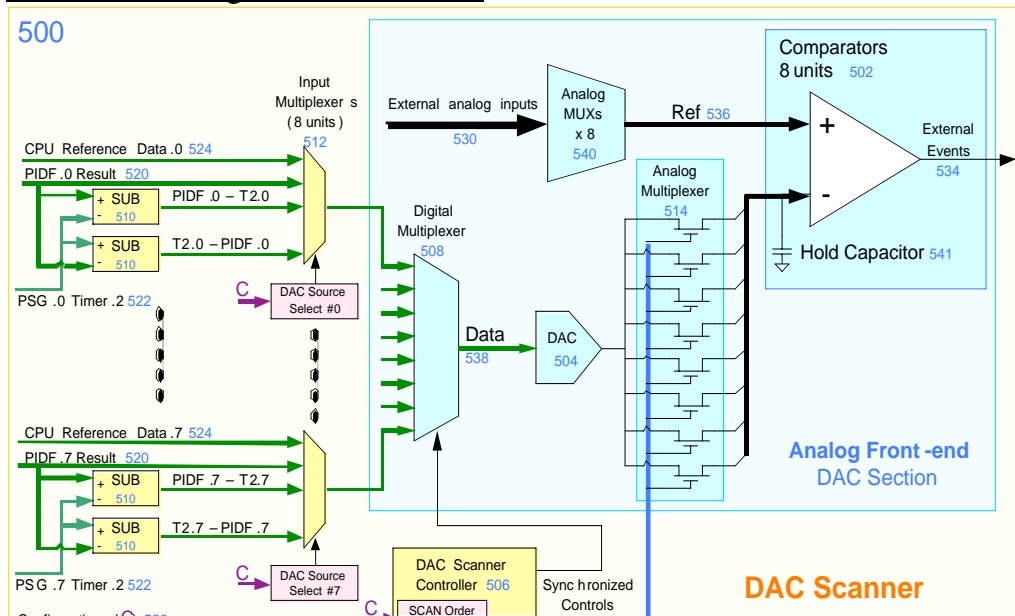
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IDC2XXX Configurable ADC Block

Abbreviation appearing in the following diagram: LUT (Look-up Table)



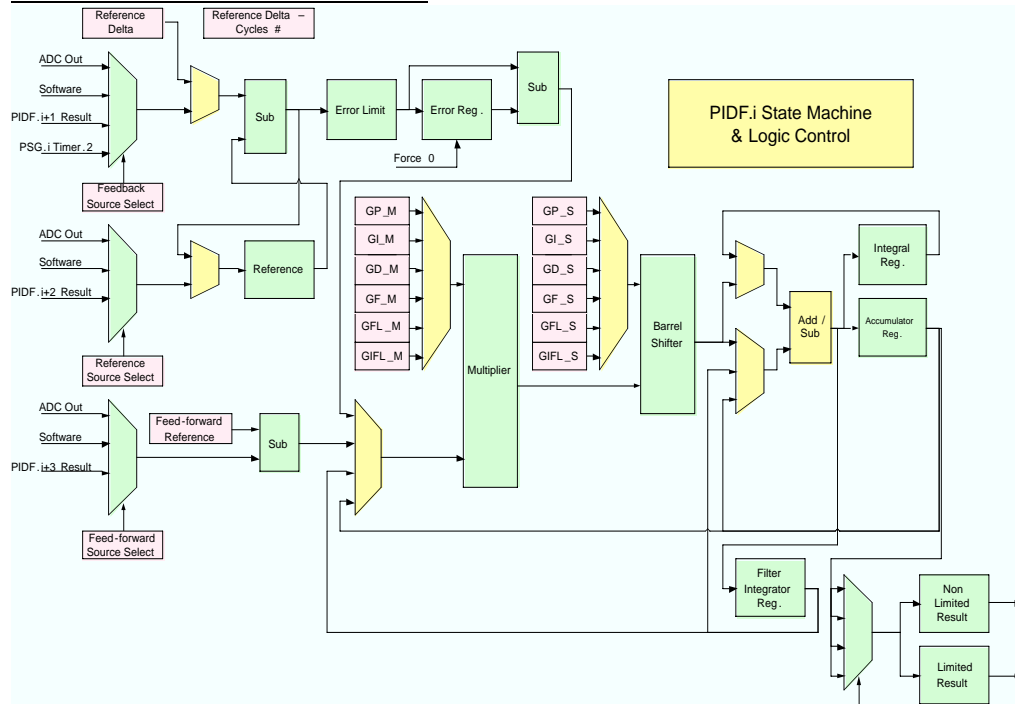
IDC2XXX Configurable DAC Block



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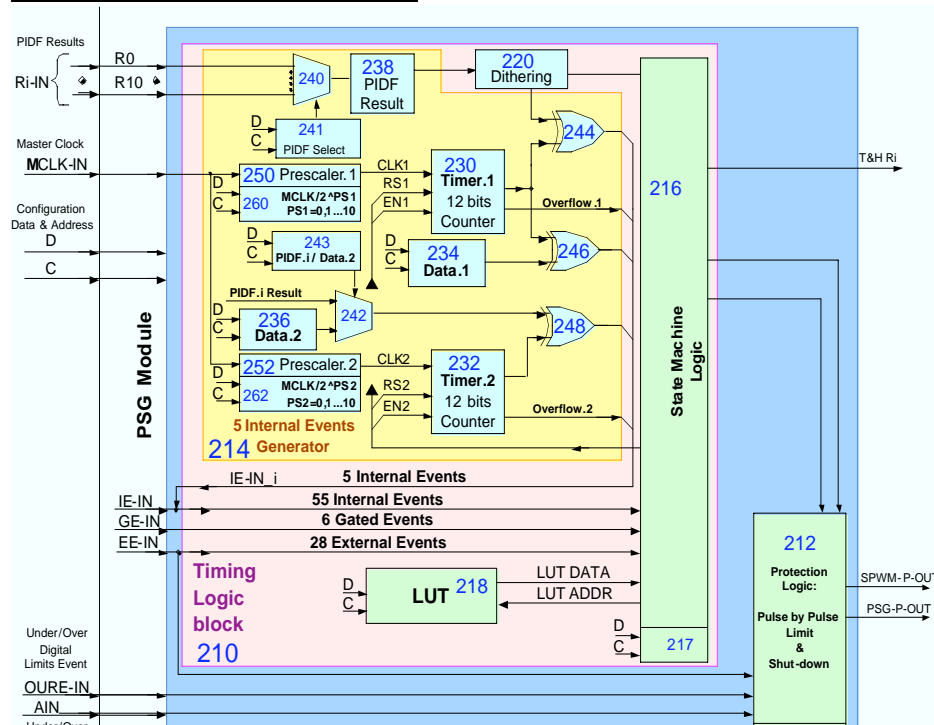
IDC2XXX PIDF Channel Block



PIDF Block Diagram Principle Explanation

The PIDF module includes 11 identical channels. Each channel is a digital PIDF calculator producing the required value of duration time for generating the sequential drive signal in order to decrease the control loop error.

IDC2XXX PSG Channel Block



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Principle Explanation

The PSG Module includes 11 identical channels. Each channel is a programmable event driven periodic state machine. Each channel has 2 outputs: PSG output for signal programmed in its LUT and SPWM (software pulse width modulation) Output for software controlled PWM. The SPWM Output also serves as a complementary output (with programmed Dead Time) to PSG Signal when the Complementary Mode is selected (for Half Bridge like drive signals). Each channel has 2 counters of 12 bits, 3 digital comparators, 2 CPU's Data Registers, 2 PIDF Result Registers. When timer value exceeds selected register compared data, an internal event is generated. Each channel creates 5 internal events. The LUT dictates the sequence of the PSG Output, the operation of the counters and the timing of hold command to T&H analog input units. One row (Address) in the LUT dictates one state of the output sequence. LUT row contains 18 bits for determining the cycle structure as described in the following implementation example.

The above briefly described configurable event driven state machine architecture enables production of almost any desired known or future requested switching drive signal or drive signals group (multi switches inverters like full bridge, three phase, multi phase and etc.). Each PSG Channel includes: Pulse by Pulse width limit driven by selected external events, Shutdown mechanism driven by Over/Under limits of selected inputs and/or predefined external events with configurable shutdown delay number of the PSG signal cycles.

CPU

The CPU task is described in the following table:

Function	Explanation
Initialization & Wake up	Wake up the SOC by loading the application configuration from flash or ROM into the Custom Logic
Communication	Communicates with external device for power management
Monitoring	Monitors analog inputs via ADC RAM for power management
Power Management	Manages the operation according to analog and digital monitoring results, communication data, various interrupts and software definitions
On-the-fly updating	On-the-fly updating of Custom Parameters according to software predefined conditions
Software protection	Software protection by shutdown of individual PSG channel
Control Involving	Involved only in relatively slow and/or sophisticated control closed loop
Software Control	Software controlled loop for relatively slow control in case of all PIDF channels already occupied, or special algorithm not possible to implement by PIDF (rare case). In both cases using PSG Channel for cycle (PWM) generation.
Software Cycle Generation and Control	Creates and controls Software generating sequential signal by using CPU Timers. (1) for very low frequency signal below PSG range. (2) in case all PSG channels are busy and only for relatively low cycle frequency and slow control loop.

Configuration Tools

IDC2XXX architecture inherently allows the designer to create his ASIC by configuring this architecture to the desired topology and algorithms without the arduous design process and without need to fabricate his own silicon.

PowerScene™ is a GUI based on a high level automatic S/W tool used during the development stage enables the designer to configure the SoC to the required application, (topology, algorithms, management).

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The PDK, a GUI design tool allows the designer to select the desired power topology and control algorithms, to create the lamp light curve database and to tune the control functions fixed parameters, thus achieving the desired performance.

Two ways to create a new application:

- I. Modification of an application having the same power topology and functional algorithms by using dedicated PDK to tune the chip to achieve the end product targeted performance.
- II. Using PowerScene™ to redefine the IDC2XXX architecture for a new power topology and/or create the desired functional algorithms. This includes the configuration of the PSG as explained above in the section “PSG Block Diagram Principle Explanation”. Afterwards, use the PDK as described above.

Lighting Applications

The IDC2XXX is a powerful digital SoC controller for lighting that integrates all the functions of a high performance networkable electronic ballast in one single chip, as well as the functions required by the master and local remote controls in building control systems. This SoC controller is configurable without need of software programming and provides an unparalleled short time-to-market. This controller comprises all the control and protection functions of the ballast and lamps including an embedded power line carrier modem. Additional optional communication interfaces provided by the IDC2000 platform are: microLan, RS485, DC control, etc. for wired remote control and local control like RF (radio frequency) and IR (infrared). It also provides interfaces for occupancy and lighting sensors, other digital and analog control I/Os and emergency mode operation. The configuration capability of this controller eliminates the need to tune the circuit by selection of passive components.

The following table comprises test results of a low cost (~\$11 components), high performance and fully featured networkable 3 lamps individually-operated ballast reference design, controlled with the IDC2000 emulator. This reference design has PLC (power line carrier) communication interface in compliance with FCC and CENELEC standards

Application example: Table of Electrical Characteristics for 1, 2 and 3xCFL26W

Light level [%]		105	101	90	77	64	47	30	20	10	5	2
DC Bus [V]		367	334	289	256	223	223	212	212	212	212	234
Input Power [W] *	3 lamps	88.2	81.7	68.6	61.3	50.6	41.1	32.5	27.0	21.3	18.1	17.6
	2 lamps	60.0	55.5	46.7	41.8	34.4	28.0	22.0	18.3	14.5	12.4	12.0
	1 lamp	31.8	30.0	26.2	24.2	20.3	16.8	13.4	11.3	9.1	7.9	7.7
PF		0.99	0.99	0.99	0.99	0.99	0.99	0.99	0.99	0.99	0.98	0.98
THD [%] (3 lamps)		1.70	1.70	1.90	1.90	2.10	1.60	2.60	3.80	5.90	6.60	6.80
Lamp Voltage [V]		81.3	85.9	100	111	123	136	147	154	159	162	163
Lamp Current [mA]		303	272	190	140	108	70	44	29.5	16	10	7.5
Peak current [mA]		960	855	566	400	305	200	125	83	48	33	21

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Table of Electrical Characteristics for 1, 2 and 3xCFL26W continued

Lamp Current CF **		1.56	1.55	1.49	1.43	1.41	1.43	1.42	1.41	1.50	1.65	1.40
Filament [V]		1.40	1.30	1.50	1.56	1.92	2.50	2.70	2.90	3.00	3.10	3.40
Light level LF ripple (mV RMS)		26	24	10	4.5	4	5	7	5	3	3.5	2.7
Flicker [%]		0.5	0.5	0.2	0.1	0.1	0.2	0.5	0.5	0.6	1.4	2.3
BEF Ballast	3 lamps	1.19	1.24	1.31	1.26	1.27	1.14	0.92	0.74	0.47	0.28	0.11
Efficacy	2 lamps	1.75	1.82	1.93	1.84	1.86	1.68	1.36	1.09	0.69	0.40	0.17
Factor	1 lamp	3.30	3.37	3.44	3.18	3.15	2.80	2.24	1.76	1.09	0.63	0.26

* Stand-by power consumption: 0.5W ** Including the line frequency component

Note: All the above measurements are carried out under 120VAC input

The following subjects describe functions, algorithms and topologies that can be mainly substantiated with the IDC2XXX and are part of the differentiators between the IDC2XXX and other controller solutions in the market for electronic ballasts and networkable electronic ballast in particular.

Programmed Start Up

Note: The following start up procedure is an example of what can be achieved by taking advantage of the IDC2XXX capability to create different sequences of regimes. Each regime comprises its own pulse width and sequence variations. Each regime is applied at the corresponding ballast operation stage, thus allowing the designer to create any desirable control algorithm.

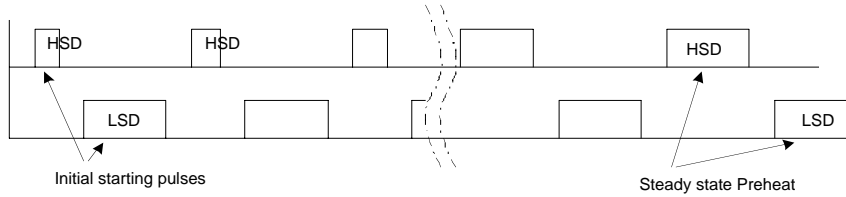
- Soft start of the Preheat stage in order to prevent a flash at start-up by gradually increasing the HSD (high side switch) pulse width until reaching the desirable pulse width which provides appropriate preheat at minimal lamp voltage. This procedure eliminates the lamp glow current during preheat. This pulse width is a pre-programmed parameter set during the ballast design.
- At the end of preheat prepare for ignition by reducing to minimum LSD (low side switch) pulse width and gradually increasing the HSD pulse width to the Ignition Value as pre-programmed parameter set during the ballast design. This procedure prevents spontaneous ignition.
- Ignite the lamp to the Ignition Light Level (pre-programmed function parameter set during ballast design) by closing the control loop on corresponding lamp current. This procedure provides controlled reliable ignition.
- On-the-fly change of control function parameters from Ignition to the lamp operation mode.
- The above program start up is implemented without the need of any passive components.
- An example of achievable (measured) start-up parameters:

Parameter	Preheat voltage	Glow current at preheat	Ignition voltage
Value	55Vrms	<1.5mArms	330Vrms 975Vpp

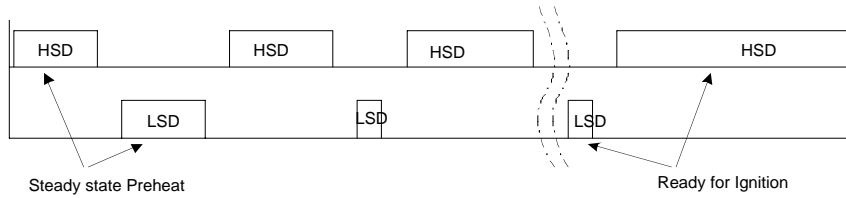
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Soft Start Preheat Regime

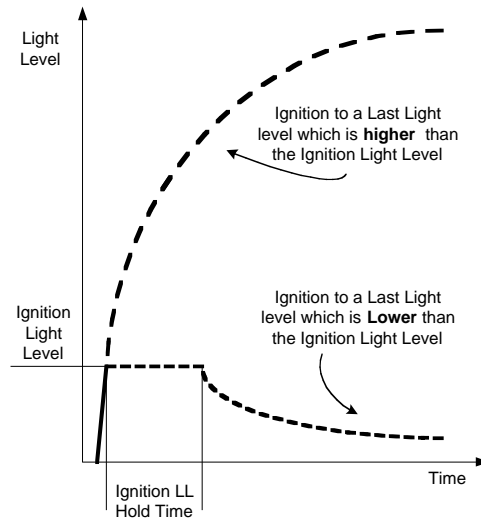


Preparation for Ignition



Ignition procedure

Ignition can be carried out in different modes. One mode is: first igniting the lamp to the Ignition Light Level (a parameter fixed during the ballast design stage) and then changing to the Last Light Level. If Last Light Level is higher than the Ignition Light Level the light will continue to climb to it at the programmed fading rate. If the Last Light Level is lower than the Ignition Light Level then the light will dim down to the Last Light Level after the Ignition Light Level Hold Time. This ensures reliable ignition to very low light levels.



Light Level Dependent Parameters [HSD, DC-Bus, THD (total harmonic distortion), Gains] -

Example

A look up table inserts different sets of parameters for 32 light levels. Parameters at every light level for: best efficiency, stable light, required filament voltage and lowest THD

Bit #	0	1	2	3	4	5	6	----->	29	30	31
Light Level (%)	1	2	4	6	8	10	13	----->	86	100	115
Lamp current (mV)	6	14	27	45	60	78	100	----->	780	1150	1500
HSD (uSec)	13	13	13	12.8	12.8	12.7	12.6	----->	12	11.5	11
DC Bus (V)	230	230	230	220	220	210	210	----->	240	250	250

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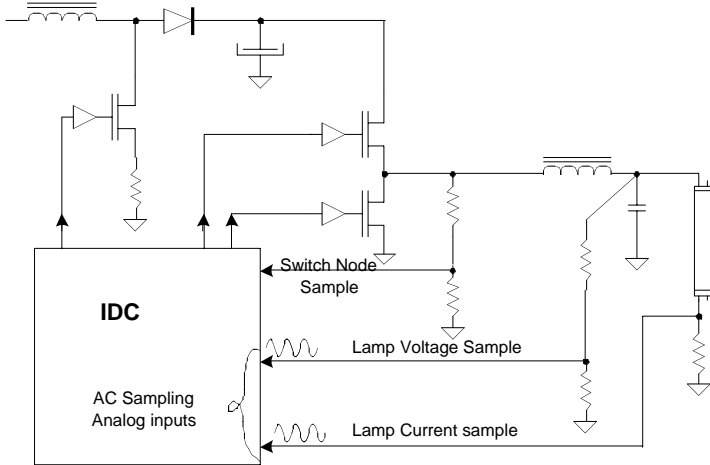
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PFC (power factor correction) On threshold current (mV)	280	280	280	280	270	270	270		190	180	180
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Note: The numbers in the Light Level and the Lamp current rows are obtained automatically from the lamp data base as created by the designer as mentioned below.

Using Lamp Current and Voltage AC Signals for control and protection functions (no need for rectification)



Lamp Instant Current and Lamp Instant Voltage are monitored several times at every HF (high frequency) cycle. This feature can provide the following benefits:

- Higher signal bandwidth
- DC information
- Lower component count
- Flexible digital filtering
- Every lamp of the system is monitored and controlled independently
- Fast protection, HV (high voltage) event is detected within the first cycle of occurrence

Dynamic dead time by sensing the half bridge switch node and applying it as an event to enable driving of half bridge switches (switch node protection)

- Zero voltage switching
- Half bridge load kept inductive
- No cross conduction currents
- Dead time interval minimized – maximizing the throughput power

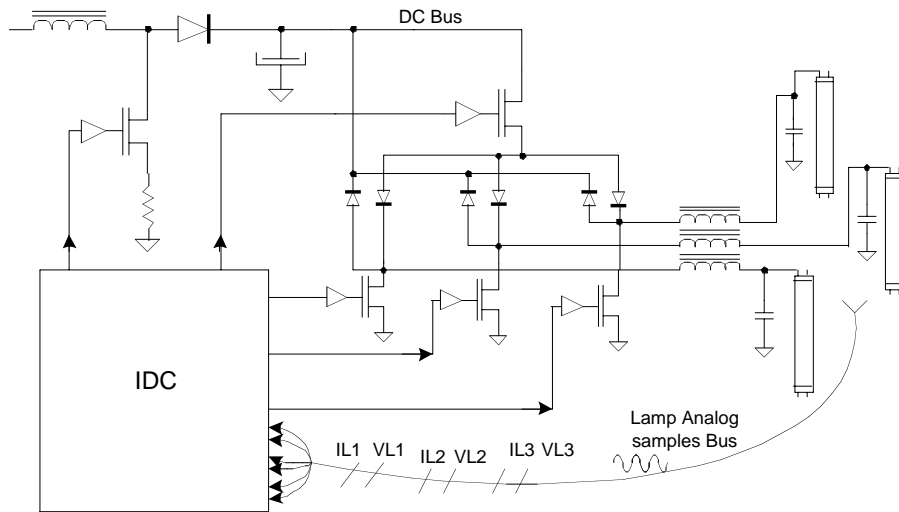
The IDC enables the use of many power topologies and many control algorithms in order to create the best required ballast.

Below is a ballast example using a novel half bridge power topology:

- One high side switch, three (>1) low side switches
- Every lamp is monitored and controlled separately
- Individual ON / OFF command is possible for every lamp
- Each lamp is protected individually – its circuit shuts down at lamp EOL (end of life)

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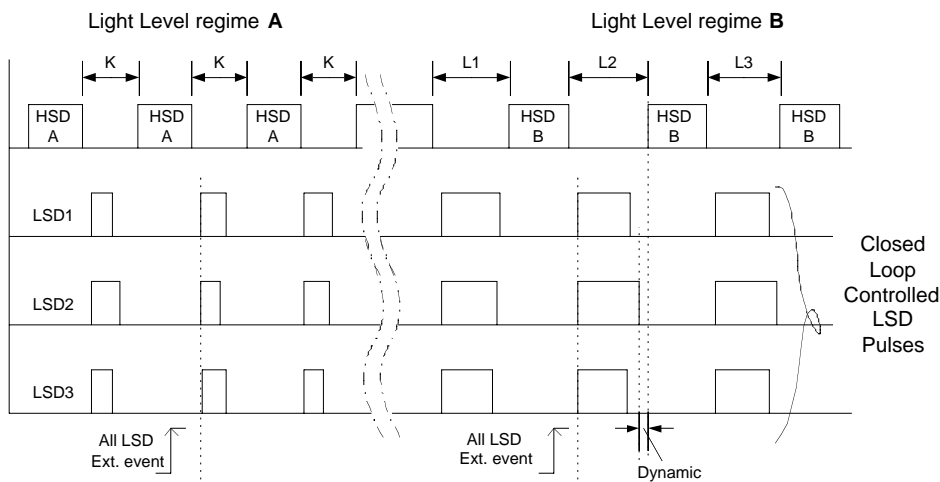
Pulse trains for two light level regimes are displayed below. These pulse trains belong to the above ballast topology and demonstrate the IDC capabilities.

HSD & LSD pulses for light level regime A:

- Open loop fixed selected HSD interval
- Dynamic dead time before activating the low sides
- Light control performed by LSD pulse width for each lamp
- Fixed K interval for low side control
- All three LSDs start together

HSD & LSD pulses for light level regime B:

- Open loop fixed selected HSD interval
- Light control performed by LSD pulse width for each lamp
- Dynamic dead time from LSD to HSD and vice versa
- Dynamic dead time from LSD to HSD starts after end of the longest LSD interval
- L1 L2 L3 intervals of regime B are dynamically created and may vary from cycle to cycle

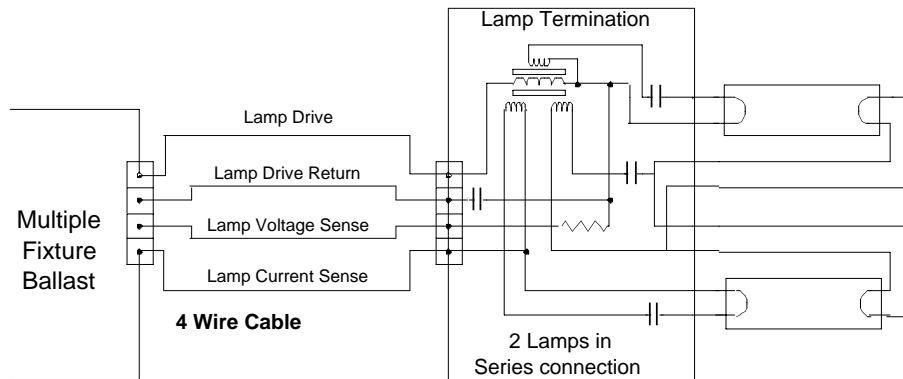


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Central ballast capabilities

The IDC is a multi channel control device. It has a configured number of output drives and analog input. This enables driving multiple light channels while controlling each one of them separately with individual voltage and current feedback per channel as depicted in figure below.



Lamps are independently controlled and protected no matter which power topology is used nor what the distance is from the ballast to the lamp fixture.

Using the above novel power topology for a central ballast, all lamps are controlled independently to one desired light level, each channel can be activated and deactivated separately, and in the case of local failure, only the bad lamp will turn off.

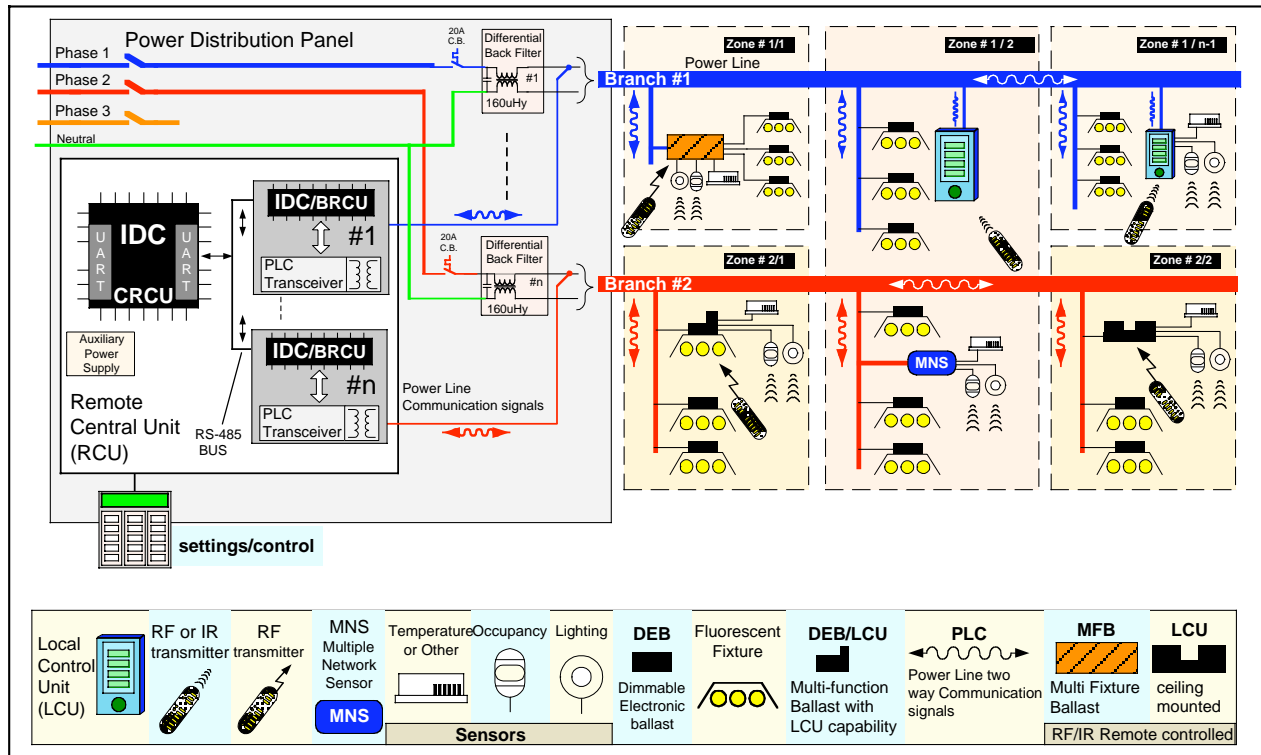
The IDC can also be configured to drive a configured number of totally independent half-bridges, where every light fixture may use a different lamp type and be controlled to a different light level.

Communication Command and Control

- Communicates bi-directionally 2 Kbits/sec rate over the power line having high reliability with a bit error rate less than 10^{-10} for a signal to noise ration of 8dB. Allows lighting commands, monitoring ballast & lamp status and sensors.
- Inherent power line communication which was designed for lighting and HVAC networking and provides all the functionality of the DALI and more at a small fraction of market solutions cost, using inherent resources of the chip.
- Capability to individually control and monitor for EOL of every single lamp of a lighting system – single or multi-fixture ballast.
- Built-in additional communication interfaces: 2.4GHz RF, 2 x UART full duplex up to 1.5 Mbit/sec
- IDC is the heart of remote controls: having PLC modem & many digital I/Os & analog inputs.

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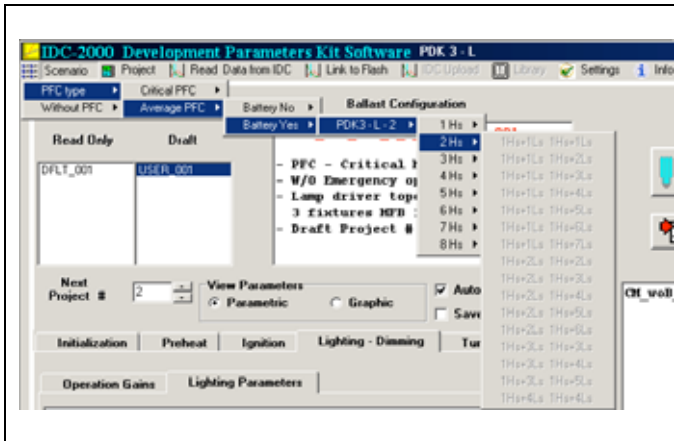


The PDK ballast design tool allows the designer to achieve the following capabilities:

- Develop a new light application: Set ballast configuration, insert ballast parameters and create (or choose from library) lamps data base using the PDK tool.
- Modify parameters to obtain best performing ballast
- Modify a large portion of the parameters on-the-fly while the ballast is operating and lamps are lit to obtain the desired performance in a matter of minutes in a fully protected environment.
- The ability to re-configure the ballast and to change all design parameters enables less hardware models, no hardware trimming, and fast new model design.
- Modify selected parameters remotely over the power line using PLC

<p>Main Screen & Ballast Configuration Configuring the desired ballast at the beginning of new design creation</p>	<p>Lamp Light Curve Screen Normalizing a particular lamp current feedback signal to lamp light level in order to use it to control lamp light</p>
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Gains Programming
 Ballast operational gains can be changed under operation for best stability

PFC Programming
 PFC parameters can be changed under operation (on the fly) for lowest THD

